Amendment to the Drawings:

Please see the attached replacement Figure 1.

Amendment to the Specification:

Please amend the paragraphs beginning at page 2 line 18 of the as-filed specification as follows:

~~As indicated in claim 2,~~ **In an embodiment** the phase lock may suitably be performed by measuring a phase difference between the recovered clock signal an the received data signal and by time delaying one of them depending on this phase difference.

~~As indicated in claim 3,~~ **In an embodiment** it may be the recovered clock signal which is time delayed depending on the measured phase difference. This provides a very exact time adjustment, and in addition it is advantageous that the time delay only has to be implemented at a single frequency since the clock signal only as a single frequency component.

Alternatively, it may, ~~as indicated in claim 4,~~ be the received data signal which is time delayed depending on the measured phase difference.

The time delay may~~, as indicated in claim 5,~~ be produced by providing the measured phase difference as steering signal to a controllable delay unit. A relatively simple solution is thus obtained in that the desired effect can be achieved with only one component, i.e. a controllable delay unit.

Alternatively, the time delay may~~, as indicated in claim 6,~~ be produced by providing the measured phase difference as a further steering signal to a frequency locked loop in which a controlled oscillator produces the recovered clock signal controlled by a signal which is produced as a measure of a frequency variation between the recovered clock signal and an output signal from said resonator circuit. By use of a frequency locked loop for producing the time delayed signal, the latter may generally be produced without jitter, causing the retimed data signal to be largely free of jitter, as well.

Please further amend the paragraphs beginning at page 3 line 20 of the as-filed specification as follows:

~~As indicated in claim 8,~~ **In an embodiment** the circuit may suitably comprise means for measuring a phase difference between the recovered clock signal and the received data signal for performing said phase lock by time delaying one of them depending on this phase difference.

~~As indicated in claim 9,~~ **In an embodiment** it may be the recovered clock signal which is time delayed depending on the measured phase difference by means comprise by the circuit. This provides a very exact time measurement, and in addition it is advantageous that the time delay only has to be implemented at a single frequency since the clock signal has only a single frequency component.

Alternatively, it may~~, as indicated in claim 10,~~ be the receive data signal which is time delayed by means comprised by the circuit depending on the measured phase difference.

The circuit may~~, as indicated by claim 11,~~ comprise a controllable delay unit for producing said time delay controlled by the measured phase difference. A relatively simple solution is thus obtained in that the desired effect can be achieved with only one component, i.e. a controllable delay unit.

Alternatively, the circuit may~~, as indicated in claim 12,~~ comprise a frequency locked loop for producing said time delay, in which loop a controlled oscillator may produce the recovered clock signal controlled by a signal which is produced as a measure of a frequency variation between the recovered clock signal and an output signal from said resonator circuit, the frequency locked loop in addition being designed to produce said time delay by application of the measured phase difference as a further steering signal to said loop. By use of a frequency locked loop for producing the time delayed signal, the latter may generally be produced without jitter, causing the retimed data signal to be largely free of jitter, as well.